

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-4, 8-12, 14-16, 18, 22-24, and 26 are pending in the application, with claims 1 and 15 being the independent claims. Claims 15 is sought to be amended. Claim 43 is sought to be cancelled. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objection to the Claims

Claims 15 and 18 were objected to for alleged informalities in the claim language. Without acquiescing to the propriety of the objection, Applicants have amended claim 15 to accommodate the objection. Accordingly, Applicants respectfully request that the objection of claims 15 and 18 be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1, 3, 4, 8-12, and 14

Claims 1, 3, 4, 8-12, and 14 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,412,064 to Wang et al. ("Wang") in view of U.S. Patent No. 6,629,179 to Bashford ("Bashford"). For the reasons set forth below, Applicants respectfully traverse.

Wang is directed to a system and method for retiring instructions issued out of order in a superscalar microprocessor system. (Wang 4:31-33.) The superscalar microprocessor system of Wang has a plurality of functional units that together can be used to execute multiple instructions in one clock cycle. (Wang 5:59-65.) The processor in Wang works well as long as there are current instructions to insert in the processor for execution that are not dependent on the “result” of an instruction yet to begin or complete execution. For example, the “result” of a conditional branch instruction determines the next set of instructions to be executed in the flow of a program. (Wang 2:12-18.) However, if the conditional branch instruction has not begun or completed execution before the next set of instructions are to be inserted into Wang’s superscalar microprocessor, there is no exact way to tell which instructions should be inserted next. (Wang 2:18-26.)

The processor described in Wang attempts to predict which way a conditional branch instruction will evaluate so that the processor does not have to stall until the conditional branch instruction has been resolved. (Wang 7:45-52.) Based on the prediction as to which way the conditional branch instruction will resolve—true or false—the processor will insert the next set of instructions *out-of-order* (i.e., before the branch instruction has completed). (*Id.*)

The superscalar microprocessor system of Wang includes an instruction retirement unit (IRU) 400, illustrated in FIG. 4, to keep track of instructions executed out-of-order and instructions executed in order to allow the microprocessor to quickly recover from an exception or a branch misprediction. (Wang 7:56-67.) The IRU 400 of Wang specifically includes a temporary buffer 403 that stores “[t]he results of all instructions executed out of order” and a register array 404 that stores all instructions

completed in order. (Wang 10:6-17.) Instructions that are completed in order are stored in register array 404 and are marked as “done” using a done flag, which indicates that the instruction is retired. (Wang 10:23-38.) Instructions completed out of order remain in temporary buffer 403 until all previous instructions are completed. (*Id.*) Once all earlier instructions are completed without any exceptions or branch mispredictions, the one or more instructions are retired by transferring the instructions from temporary buffer 403 to register array 404 and there associated done flags are marked “done.” (*Id.*)

The Examiner appears to contend that this transferring of instructions from temporary buffer 403 to register array 404 in Wang, is equivalent to the feature:

if processing of the first data completes before processing of the second data completes and the first control record is younger than the second control record, moving a first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record, wherein moving the first interrupt indicator comprises ***setting the first interrupt indicator associated with the first control record to disabled and setting the second interrupt indicator associated with the second control record to enabled . . .***

as recited in Applicants’ claim 1.

Even if we assume for the sake of argument that the done flags disclosed in Wang are comparable to the interrupt indicators recited in claim 1, Wang does not disclose a two-step moving process where a done flag associated with one instruction is set to disabled (i.e., not “done”) and a done flag associated with another instruction is set to enabled (i.e., “done”), if processing of the one instruction completes before the other.

Rather, and at most, Wang discloses, in a first scenario, that a completed instruction is stored in temporary buffer 403 and is ***not*** marked as “done” because an earlier instruction has not been completed and is further ***not*** marked as “done.”

However, in a second scenario, Wang discloses that the instruction, stored in temporary buffer 403 and waiting for the earlier instruction to be completed, can be transferred to register array 404 and marked as “done” once the earlier instruction is stored in register array 404 and marked as “done”. Thus, in both of these scenarios disclosed in Wang, the two instructions are either both marked as “done” or are marked as not “done.”

Thus, Wang does not disclose “wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the first control record to *disabled* and setting the second interrupt indicator associated with the second control record to *enabled*” as recited in claim 1. The moving process recited in claim 1 occurs “if processing of the first data completes before processing of the second data completes and the first control record is younger than the second control record” as further recited in claim 1.

Bashford do not cure the deficiencies of Wang. For the reasons set forth above, the combination of Wang and Bashford cannot render claim 1 unpatentable. Claims 3, 4, 8-12, and 14 are similarly not rendered unpatentable by the combination of Wang and Bashford for the same reasons as independent claim 1, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 1, 3, 4, 6-12, and 14 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 2, 15, 16, 18, 22-24, 26, and 23

Claims 2, 15, 16, 18, 22-24, 26, and 43 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wang in view of Bashford and in further view of

Pierson et al., “Context-Agile Encryption for High Speed Communication Networks” (“Pierson”). For the reasons set forth below, Applicants respectfully traverse.

Pierson does not in anyway remedy the deficiencies of Wang and Bashford with respect to independent claim 1, as discusses above. Consequently, the combination of Wang, Bashford, and Pierson cannot render independent claim 1 unpatentable. Claim 2 is similarly not rendered unpatentable by the combination of Wang, Bashford, and Pierson for the same reasons as independent claim 1, from which it depends, and further in view of its own respective feature. Accordingly, Applicants respectfully request that the rejection of claim 2 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 15 recites, among other features “wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the first control record to disabled and setting the second interrupt indicator associated with the second control record to enabled.” As noted above in regard to claim 1, Wang, Bashford do not teach or suggest such a feature. Pierson does not cure the deficiencies of Wang and Bashford. Consequently, the combination of Wang, Bashford, and Pierson cannot render independent claim 15 unpatentable. Claims 16, 18, 22-24, and 26 are similarly not rendered unpatentable by the combination of Wang, Bashford, and Pierson for the same reasons as independent claim 15, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 15-18, 22-24, and 26 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

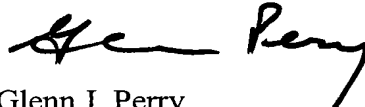
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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